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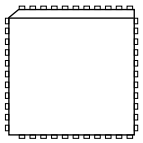
3935

Data Sheet
26301.102b

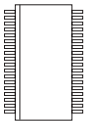
3-PHASE POWER MOSFET CONTROLLER — For Automotive Applications

Package ED, 44-Pin PLCC



Package JP, 48-Pin LQFP

Package LQ, 36-Pin SOIC



ABSOLUTE MAXIMUM RATINGS

Load Supply Voltages, VBAT, VDRAIN, VBOOST, BOOSTD ... **-0.6 V to 40 V**

Output Voltage Ranges,
- GHA/GHB/GHC, V_{GHX} .. **-4 V to 55 V**
- SA/SB/SC, V_{SX} ..... **-4 V to 40 V**
- GLA/GLB/GLC, V_{GLX} .... **-4 V to 16 V**
- CA/CB/CC, V_{CX} ..... **-0.6 V to 55 V**

Sense Circuit Voltages,
- CSP,CSN, LSS ..... **-4 V to 6.5 V**

Logic Supply Voltage,
- V_{DD} ..... **-0.3 V to +6.5 V**

Logic Input/Outputs and OVSET, BOOSTS, CSOUT, VDSTH ..... **-0.3 V to 6.5 V**

Operating Temperature Range,
- T_A ..... **-40°C to +135°C**

Junction Temperature, T_J ..... **+150°C**

Storage Temperature Range,
- T_S ..... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The A3935 is designed specifically for automotive applications that require high-power motors. Each provides six high-current gate drive outputs capable of driving a wide range of n-channel power MOSFETs.

A requirement of automotive systems is steady operation over a varying battery input range. The A3935 integrates a pulse-frequency modulated boost converter to create a constant supply voltage for driving the external MOSFETs. Bootstrap capacitors are utilized to provide the above battery supply voltage required for n-channel FETs.

Direct control of each gate output is possible via six TTL-compatible inputs. A differential amplifier is integrated to allow accurate measurement of the current in the three-phase bridge.

Diagnostic outputs can be continuously monitored to protect the driver from short-to-battery, short-to-supply, bridge-open, and battery under/overvoltage conditions. Additional protection features include dead-time, VDD undervoltage, and thermal shutdown.

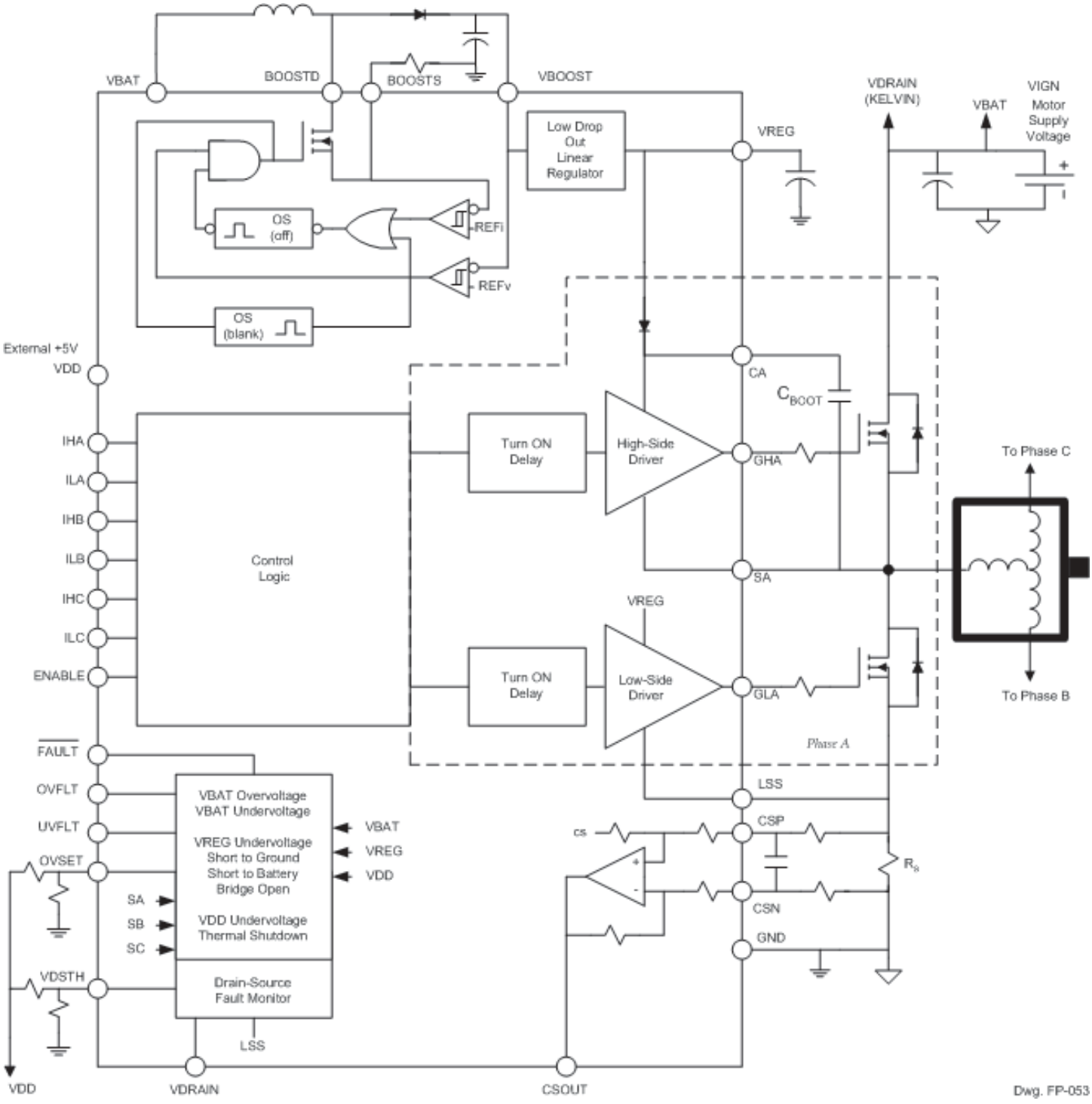
The A3935 is supplied in a choice of three packages, a 44-lead PLCC with copper batwing tabs (suffix ED), a 48-lead low profile QFP with exposed thermal pad (suffix JP), and a 36-lead 0.8 mm pitch SOIC (suffix LQ).

FEATURES

- Drives wide range of n-channel MOSFETs in 3-phase bridges
- PFM boost converter for use with low-voltage battery supplies
- Internal LDO regulator for gate-driver supply
- Bootstrap circuits for high-side gate drivers
- Current monitor output
- Adjustable battery overvoltage detection.
- Diagnostic outputs
- Motor lead short-to-battery, short-to-ground, and bridge-open protection
- Undervoltage protection
- -40 °C to +150 °C, T_J operation
- Thermal shutdown

Always order by complete part number, e.g., **A3935KLQ**.

Functional Block Diagram



See pages 8 and 9 for terminal assignments and descriptions.

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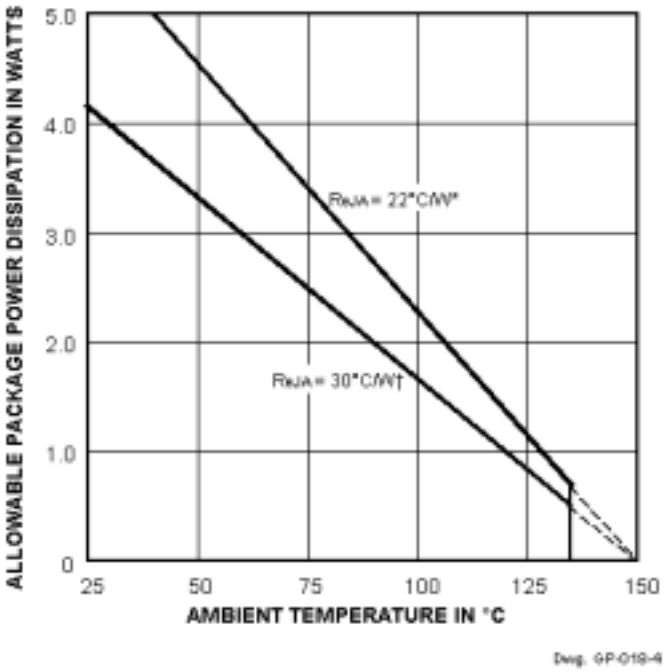
A3935KED (PLCC)



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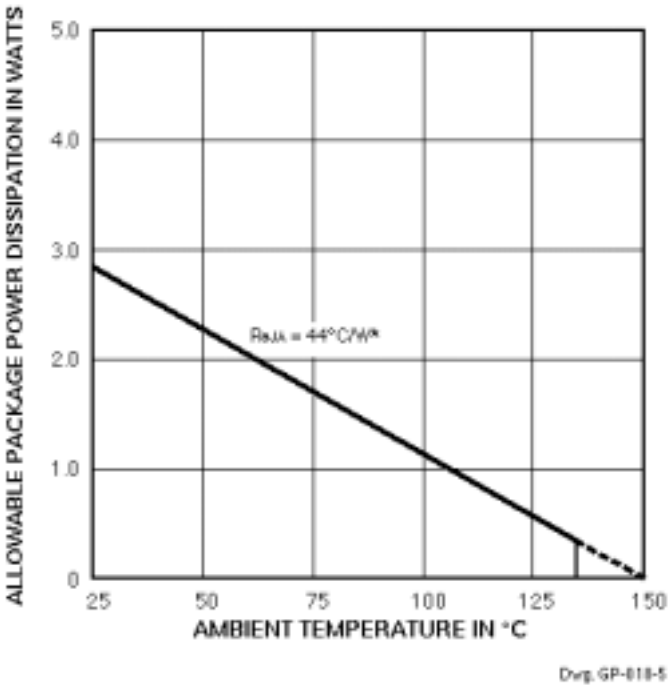
A3935KLQ (SOIC)



Dwg. GP-018-5

* Measured on “High-K” multi-layer PWB per JEDEC Standard JESD51-7.

† Measured on typical two-sided PWB with power tabs (terminals 1, 2, 11, 12, 22, 23, 34, and 35) connected to copper foil with an area of 3.8 square inches (2452 mm^2) on each side. See Application Note 29501.5, *Improving Batwing Power Dissipation*, for additional information.

ELECTRICAL CHARACTERISTICS: unless otherwise noted at T_J = -40°C to +150°C, V_{BAT} = 7 V to 16 V, V_{DD} = 4.75 V to 5.25 V, ENABLE = 22.5 kHz, 50% Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Power Supply						
V_{DD} Supply Current	I_{DD}	All logic inputs = 0 V	–	–	7.0	mA
V_{BAT} Supply Current	I_{BAT}	All logic inputs = 0 V	–	–	3.0	mA
Battery Voltage Operating Range	V_{BAT}		7.0	–	40	V
Bootstrap Diode Forward Voltage	V_{DBOOT}	$I_{DBOOT} = -I_{cx}$ = 10 mA, $V_{DBOOT} = V_{REG} - V_{CX}$	0.8	–	2.0	V
		$I_{DBOOT} = -I_{cx}$ = 100 mA	1.5	–	2.3	V
Bootstrap Diode Resistance	r_{DBOOT}	r_D(100 mA) = [V_D(150 mA) – V_D(50 mA)]/100 mA	2.5	–	7.5	Ω
Bootstrap Diode Current Limit	I_{DM}	3 V < [$V_{REG} - V_{CX}$] < 12 V	-150	–	-1150	mA
Bootstrap Quiescent Current	I_{CX}	V_{CX} = 40 V, GHx = ON	10	–	30	µA
Bootstrap Refresh Time	$t_{refresh}$	V_{SX} = low to guarantee ΔV = +0.5 V refresh of 0.47 µF Boot Cap at $V_{cx} - V_{sx}$ = +10 V	–	–	2.0	µs
VREG Output Voltage [1]	V_{REG}	V_{BAT} = 7 V to 40 V, V_{BOOST} from Boost Reg	12.7	–	14	V
VREG Dropout Voltage [2]	V_{REGDO}	$V_{REGDO} = V_{boost} - V_{reg}$, I_{reg} = 40 mA	–	0.9	–	V
Gate Drive Avg. Supply Current	I_{REG}	No external dc load at VREG, C_{REG} = 10 µF	–	–	40	mA
VREG Input Bias Current	$I_{REGBIAS}$	Current into V_{BOOST}, ENABLE = 0	–	–	4.0	mA
Boost Supply						
V_{BOOST} Output Voltage Limit	V_{BOOSTM}	V_{BAT} = 7 V	14.9	–	16.3	V
V_{BOOST} Output Volt. Limit Hyst.	ΔV_{BOOSTM}		35	–	180	mV
Boost Switch ON Resistance	$r_{DS(on)}$	I_{BOOSTD} < 300 mA	–	1.4	3.3	Ω
Max. Boost Switch Current	$I_{BOOSTSW}$		–	–	300	mA
Boost Current Limit Threshold Volt.	$V_{BI(th)}$	Increasing V_{BOOSTS}	0.45	–	0.55	V
OFF Time	t_{off}		3.0	–	8.0	µs
Blanking Time	t_{blank}		100	–	220	ns

NOTES: Typical Data and Typical Characteristics are for design information only.
Negative current is defined as coming out of (sourcing) the specified device terminal.
1. For $V_{BOOSTM} < V_{BOOST} < 40$ V power dissipation in the V_{REG} LDO increases. Observe $T_J < 150$ °C limit.
2. With V_{BOOST} decreasing Dropout Voltage measured at $V_{REG} = V_{REGref} - 200$ mV where $V_{REG(ref)} = V_{REG}$ at V_{BOOST} = 16 V.

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Continued next page …

ELECTRICAL CHARACTERISTICS: unless otherwise noted at T_J = -40°C to +150°C, V_{BAT} = 7 V to 16 V, V_{DD} = 4.75 V to 5.25 V, ENABLE = 22.5 kHz, 50% Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Control Logic						
Logic Input Voltages	$V_{I(1)}$	Minimum high level input for logical “one”	2.0	–	–	V
	$V_{I(0)}$	Maximum low level input for logical “zero”	–	–	0.8	V
Logic Input Currents	$I_{I(1)}$	$V_I = V_{DD}$	–	–	500	µA
	$I_{I(0)}$	V_I = 0.8 V	50	–	–	µA
Input Hysteresis	V_{hys}		100	–	300	mV
Logic Output High Voltage	$V_{O(H)}$	$I_{O(H)}$ = -800 µA	V_{DD}–0.8	–	–	V
Logic Output Low Voltage	$V_{I(L)}$	$I_{O(L)}$ = 1.6 mA	–	–	0.4	V
Gate Drives, GHx (internal SOURCE or upper switch stages)						
Output High Voltage	$V_{DSL(H)}$	GHx: I_{xU} = –10 mA, V_{sx} = 0	V_{REG}–2.26	–	V_{REG}	V
		GLx: I_{xU} = –10 mA, V_{lss} = 0	V_{REG}–0.26	–	V_{REG}	V
Source Current (pulsed)	I_{xU}	V_{SDU} = 10 V, T_J = 25 °C	–	800	–	mA
		V_{SDU} = 10 V, T_J = 135 °C	400	–	–	mA
Source ON Resistance	$r_{SDU(on)}$	I_{xU} = –150 mA, T_J = 25 °C	4.0	–	10	Ω
		I_{xU} = –150 mA, T_J = 35 °C	7.0	–	15	Ω
Gate Drives, GLx (internal SINK or lower switch stages)						
Sink Current (pulsed)	I_{xL}	V_{DSL} = 10 V, T_J = 25 °C	–	850	–	mA
		V_{DSL} = 10 V, T_J = 135 °C	550	–	–	mA
Sink ON Resistance	$r_{DSL(on)}$	I_{xL} = +150 mA, T_J = 25 °C	1.8	–	6.0	Ω
		I_{xL} = +150 mA, T_J = 135 °C	3.0	–	7.5	Ω
Gate Drives, GHx, GLx (General)						
Phase Leakage (Source)	I_{Sx}	ENABLE = 0, V_{Sx} = 1.7 V	0	–	100	µA
Propagation Delay, Logic only	t_{pd}	Logic input to unloaded GHx, GLx	–	–	150	ns
Output Skew Time	$t_{sk(o)}$	Grouped by edge, phase-to-phase	–	–	50	ns
Dead Time (Shoot-Through Prevention)	t_{dead}	Between GHx, GLx transitions of same phase	75	–	180	ns

NOTES: Typical Data and Typical Characteristics are for design information only.
Negative current is defined as coming out of (sourcing) the specified device terminal.
For GH_X: $V_{SDU} = V_{CX} – V_{GHX}$, $V_{DSL} = V_{GHX} – V_{SX}$, $V_{DSL(H)} = V_{CX} – V_{SDU} – V_{SX}$.
For GL_X: $V_{SDU} = V_{REG} – V_{GLX}$, $V_{DSL} = V_{GLX} – V_{LSS}$, $V_{DSL(H)} = V_{REG} – V_{SDU} – V_{LSS}$.

ELECTRICAL CHARACTERISTICS: unless otherwise noted at T_J = -40°C to +150°C, V_{BAT} = 7 V to 16 V, V_{DD} = 4.75 V to 5.25 V, ENABLE = 22.5 kHz, 50% Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Sense Amplifier						
Input Bias Current	I_{bias}	CSP = CSN = 0 V	-180	–	-360	µA
Input Offset Current	I_{IO}	CSP = CSN = 0 V	–	–	±35	µA
Input Resistance	r_i	CSP with respect to GND	–	80	–	kΩ
		CSN with respect to GND	–	4.0	–	kΩ
Diff. Input Operating Voltage	V_{ID}	V_{ID} = CSP – CSN, -1.3V < CSP,N < 4V	–	–	±200	mV
Output Offset Voltage	V_{OO}	CSP = CSN = 0 V	77	250	450	mV
Output Offset Voltage Drift	ΔV_{OO}	CSP = CSN = 0 V	–	100	–	µV/°C
Input Com-Mode Oper. Range	V_{IC}	CSP = CSN	-1.5	–	4.0	V
Voltage Gain	A_V	V_{ID} = 40 mV to 200 mV	18.6	19.2	19.8	V/V
Low Output Voltage Error	E_v	V_{id} = 0 to 40 mV, V_o = (19.2 x V_{ID}) + V_o + E_v	–	–	±25	mV
DC Common-Mode Attenuation	A_{VC}	CSP = CSN = 200 mV	28	–	–	dB
Output Resistance	r_o	V_{CSOUT} = 2.0 V	–	8.0	–	Ω
Output Dynamic Range	V_{CSOUT}	I_{CSOUT} = -100 µA at top rail, 100 µA at bottom rail	0.075	–	V_{DD}-0.25	V
Output Current, Sink	I_{sink}	V_{CSOUT} = 2.5 V	20	–	–	mA
Output Current, Source	I_{source}	V_{CSOUT} = 2.5 V	-1.0	–	–	mA
VDD Supply Ripple Rejection	PSRR	CSP = CSN = GND, freq. = 0 to 1 MHz	20	–	–	dB
VREG Supply Ripple Rejection	PSRR	CSP = CSN = GND, freq. = 0 to 300 kHz	45	–	–	dB
Small Signal 3-dB Bandwidth	f_{3db}	10 mV input	–	1.6	–	MHz
AC Common-Mode Attenuation	A_{vc}	V_{cm} = 250 mV/pp, freq. = 0 to 800 kHz	26	–	–	dB
Output Slew Rate (positive or negative)	SR	200 mV step input, meas. 10/90% points	10	–	–	V/µs

NOTES: Typical Data and Typical Characteristics are for design information only.
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Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Fault Logic						
VDD Undervoltage	$V_{DD(uv)}$	Decreasing V_{DD}	3.8	–	4.3	V
VDD Undervoltage Hysteresis	$\Delta V_{DD(uv)}$	$V_{DD(recovery)}$ - $V_{DD(uv)}$	100	–	300	mV
OVSET Operating Volt. Range	$V_{SET(ov)}$		0	–	V_{DD}	V
OVSET Calibrated Volt. Range	$V_{SET(ov)}$		0	–	2.5	V
OVSET Input Current Range	$I_{SET(ov)}$		-1.0	–	+1.0	µA
VBAT Overvoltage Range	$V_{BAT(ov)}$	0 V < $V_{SET(ov)}$ < 2.5 V	19.4	–	40	V
VBAT Overvoltage	$V_{BAT(ov)}$	Increasing V_{BAT}, $V_{SET(ov)}$ = 0 V	19.4	22.4	25.4	V
VBAT Overvoltage Hysteresis	$\Delta V_{BAT(ov)}$	Percent of $V_{BAT(ov)}$ value set by $V_{SET(ov)}$	9.0	–	15	%
VBAT Overvoltage Gain Constant	$K_{BAT(ov)}$	$V_{BAT(ov)} = (K_{BAT(ov)} \times V_{SET(ov)}) + V_{BAT(ov)}$ [0]	–	12	–	V/V
VBAT Undervoltage	$V_{BAT(uv)}$	Decreasing V_{BAT}	5.0	5.25	5.5	V
VBAT Undervoltage Hysteresis	$\Delta V_{BAT(uv)}$	Percent of $V_{BAT(uv)}$	8.0	–	12	%
VREG Undervoltage	$V_{REG(uv)}$	Decreasing V_{REG}	9.9	–	11.1	V
VDSTH Input Range	V_{DSTH}		0.5	–	3.0	V
VDSTH Input Current	I_{DSTH}	V_{DSTH} > 0.8 V	40	–	100	µA
Short-to-Ground Threshold	$V_{STG(th)}$	With a high-side driver “on”, as V_{SX} decreases, V_{DRAIN} - V_{SX} > V_{STG} causes a fault	V_{DSTH}-0.3	–	V_{DSTH}+0.2	V
Short-to-Battery Threshold	$V_{STB(th)}$	With a low-side driver “on”, as V_{SX} increases, V_{SX} - V_{LSS} > V_{STB} causes a fault	V_{DSTH}-0.3	–	V_{DSTH}+0.2	V
V_{DRAIN}/Open Bridge Oper. Range	V_{DRAIN}	7 V < V_{BAT} < 40 V	-0.3	–	V_{BAT}+2.0	V
V_{DRAIN}/Open Bridge Current	I_{VDRAIN}	7 V < V_{BAT} < 40 V	0	–	1.0	mA
V_{DRAIN}/Open Bridge Threshold Volt.	$V_{BDGO(th)}$	If V_{DRAIN} < V_{BDGOTH} then a bridge fault occurs	1.0	–	3.0	V
Thermal Shutdown Temp.	T_J		160	170	180	°C
Thermal Shutdown Hysteresis	ΔT_J		7.0	10	13	°C

NOTES: Typical Data and Typical Characteristics are for design information only.
Negative current is defined as coming out of (sourcing) the specified device terminal.

Terminal Functions

Terminal Name	Function	A3935KED (PLCC)	A3935KJP (QLFP)	A3935KLQ (SOIC)
CSP	Current-sense input, positive-side	31	19	1
VDSTH	DC input, drain-to-source monitor threshold voltage	32	20	2
LSS	Gate-drive source return, low-side	33	21	3
GLC	Gate-drive C output, low-side	36	22	4
SC	Load phase C input	37	26	5
GHC	Gate-drive C output, high-side	38	27	6
CC	Bootstrap capacitor C	39	28	7
GLB	Gate-drive B output, low-side	40	29	8
SB	Load phase B input	41	30	9
GHB	Gate-drive B output, high-side	42	31	10
CB	Bootstrap capacitor B	43	32	11
GLA	Gate-drive A output, low-side	44	33	12
SA	Load phase A input	3	34	13
GHA	Gate-drive A output, high-side	4	38	14
CA	Bootstrap capacitor A	5	39	15
VREG	Gate drive supply, positive	6	40	16
VDRAIN	Kelvin connection to MOSFET high-side drains	7	41	17
VBOOST	Boost supply output	8	42	18
BOOSTS	Boost switch, source	9	43	19
BOOSTD	Boost switch, drain	10	44	20
VBAT	Battery supply, positive	13	46	22
UVFLT	VBAT undervoltage fault output	14	3	23
OVFLT	VBAT overvoltage fault output	15	4	24
$\overline{\text{FAULT}}$	Active-low fault output, primary	16	5	25
ALO	Gate control input A, low-side	17	6	26
AHI	Gate control input A, high-side	18	7	27
BHI	Gate control input B, high-side	19	8	28
BLO	Gate control input B, low-side	20	9	29
CLO	Gate control input C, low-side	21	10	30
CHI	Gate control input C, high-side	24	11	31
ENABLE	Gate output enable	25	12	32
OVSET	DC input, overvoltage threshold setting for VBAT	26	15	33
NC	Not connected, no external connection allowed	27	1,2,13,14,23,24, 25,35,36,37,47,48	–
CSOUT	Current-sense amplifier output	28	16	34
VDD	Logic supply, nominally +5 V	29	17	35
CSN	Current-sense input, negative-side	30	18	36
GND	Ground, dc supply returns, negative, and (for ED package) heat sink tab	1, 2, 11, 12, 22, 23, 34, 35	45	21

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Terminal Descriptions

AHI/BHI/CHI. Direct control of high-side gate outputs GHA/GHB/GHC. Logic "1" drives the gate "on". Logic "0" pulls the gate down, turning off the external power MOSFET. Internally pulled down when terminal is open.

ALO/BLO/CLO. Direct control of low-side gate outputs GLA/GLB/GLC. Logic "1" drives the gate "on". Logic "0" pulls the gate down, turning off the external power MOSFET**.** Internally pulled down when terminal is open.

BOOSTD. Boost converter switch drain connection**.**

BOOSTS. Boost converter switch source connection.

CA/CB/CC. High-side connection for bootstrap capacitor, positive supply for high-side gate drive. The bootstrap capacitor is charged to VREG when the output Sx terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for n-channel power MOSFETs.

CSN. Input for current-sense, differential amplifier, inverting, negative side. Kelvin connection for ground side of current-sense resistor.

CSOUT. Amplifier output voltage proportional to current sensed across an external low-value resistor placed in the ground-side of the power FET bridge.

CSP. Input for current-sense differential amplifier, non-inverting, positive side. Connected to positive side of sense resistor.

ENABLE. Logic "0" disables the gate control signals and switches off all the gate drivers "low" causing a "coast". Can be used in conjunction with the gate inputs to PWM the load current. Internally pulled down when terminal is open.

$\overline{\text{FAULT}}$. Diagnostic logic output signal, when "low" indicates that one or more fault condition have occurred.

GHA/GHB/GHC. High-side gate-drive outputs for n-channel MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate; thereby, controlling the di/dt and dv/dt of Sx outputs.

GLA/GLB/GLC. Low-side gate drive outputs for external, n-channel MOSFET drivers. External series gate resistors can control slew rate.

GND. Ground or negative side of VDD and VBAT supplies.

LSS. Low-side gate driver returns. Connects to the common sources in the low-side of the power MOSFET bridge.

OVFLT. Logic "1" means that the VBAT exceeded the VBAT overvoltage trip point set by OVSET level. It will recover after a hysteresis below that maximum value. Normally has a high-impedance state.

OVSET. A positive, dc level that controls the VBAT overvoltage trip point. Usually, provided from precision resistor divider network between V_{DD} and GND, but can be held grounded for a preset value. When terminal is open, sets unspecified but high overvoltage trip point.

SA/SB/SC. Directly connected to the motor terminals, these terminals sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors. Also, are the negative supply connection for the floating, high-side drivers.

UVFLT. Logic "1" means that VBAT is below its minimum value and will recover after a hysteresis above that minimum value. Has a high-impedance state. [If UVFLT and OVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.]

VBAT. Battery voltage, positive input and is usually connected to the motor voltage supply.

VBOOST. Boost converter output, nominally 16 V, is also input to regulator for VREG. Has internal boost current and boost voltage control loops. In high-voltage systems is approximately one diode drop below V_{BAT}.

VDD. Logic supply, nominally +5 V.

VDRAIN. Kelvin connection for drain-to-source voltage monitor and is connected to high-side drains of MOSFET bridge. High impedance when terminal is open and registers as a short-to-ground fault on all motor phases.

VDSTH. A positive, dc level that sets the drain-to-source monitor threshold voltage. Internally pulled down when terminal is open.

VREG. High-side, gate-driver supply, nominally, 13.5 V. Has low-voltage dropout (LDO) feature.

Functional Description

Motor Lead Protection. A fault detection circuit monitors the voltage across the drain to source of the external MOSFETs. A fault is asserted "low" on the output terminal, $\overline{\text{FAULT}}$, if the drain-to-source voltage of any MOSFET that is instructed to turn on is greater than the voltage applied to the V_{DSTH} input terminal. When a high-side switch is turned on, the voltage from V_{DRAIN} to the appropriate motor phase output, V_{SX}, is examined. If the motor lead is shorted to ground before the high side is turned on, the measured voltage will exceed the threshold and the $\overline{\text{FAULT}}$ terminal will go "low". Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS terminal (source) is monitored. V_{DSTH} is set by a resistor divider to V_{DD}.

The V_{DRAIN} is intended to be a Kelvin connection for the high-side, drain-source monitor circuit. Voltage drops across the power bus are eliminated by connecting an isolated PCB trace from the V_{DRAIN} terminal to the drain of the MOSFET bridge. This allows improved accuracy in setting the V_{DSTH} threshold voltage. The low-side, drain-source monitor uses the LSS terminal, rather than V_{DRAIN}, in comparing against V_{DSTH}. The A3935 merely reports these motor faults.

Fault Outputs. Transient faults on any of the fault outputs are to be expected during switching and will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

$\overline{\text{FAULT}}$. This terminal will go active "low" when any of the following conditions occur:

V_{BAT} overvoltage,
V_{BAT} undervoltage,
V_{REG} undervoltage,
Motor lead short-to-ground,
Motor lead short-to-supply (or battery),
Bridge (or V_{DRAIN}) open,
V_{DD} undervoltage, or
Thermal shutdown.

OVFLT. Asserts "high" when a V_{BAT} overvoltage fault occurs and resets "low" after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or V_{DD} undervoltage occurs. The voltage at the OVSET terminal, V_{OVSET}, controls the V_{BAT} overvoltage set point $V_{BAT(ov)}$, i.e.,

$$V_{BAT(ov)} = (K_{BAT(ov)} \times V_{SET(ov)}) + V_{BAT(ov)}(0),$$

where $K_{BAT(ov)}$ is the gain (12) and $V_{BAT(ov)}(0)$ is the value of $V_{BAT(ov)}$ when $V_{SET(ov)}$ is zero (~22.4). For valid formula, all variables must be in range and below maximum operating specification.

UVFLT. Asserts "high" when a V_{BAT} undervoltage fault occurs and resets "low" after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or V_{DD} undervoltage occurs. OVFLT and UVFLT are mutually exclusive by definition.

Current Sensing. A current-sense amplifier is provided to allow system monitoring of the load current. The differential amplifier inputs are intended to be Kelvin connected across a low-value sense resistor or current shunt. The output voltage is represented by:

$$V_{CSOUT} = (I_{LOAD} \times A_V \times R_S) + V_{OS}$$

where V_{OS} is the output voltage calibrated at zero load current and A_V is the differential amplifier gain of about 19.2. If either the CSP or CSN pin is open, the CSOUT pin will go to its maximum positive level.

Shutdown. If a fault occurs because of excessive junction temperature or undervoltage on V_{DD} or V_{BAT}, all gate driver outputs are driven "low" until the fault condition is removed. In addition, the boost supply switch and the VREG are turned "off" until those undervoltages and junction temperatures recover.

Boost Supply. V_{BOOST} is controlled by an inner current-control loop, and by an outer voltage-feedback loop. The current-control loop turns "off" the boost switch for 5 µs whenever the voltage across the boost current-sense resistor exceeds 500 mV. A diode reverse-recovery current flows through the sense resistor whenever the boost switch turns "on", which could turn it "off" again if not for the "blanking time" circuit. Adjustment of this external sense resistor determines the maximum current in the inductor. Whenever V_{BOOST} exceeds the predefined threshold, nominally 16 V, the boost switch is inhibited.

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Functional Description (cont'd)

Input Logic

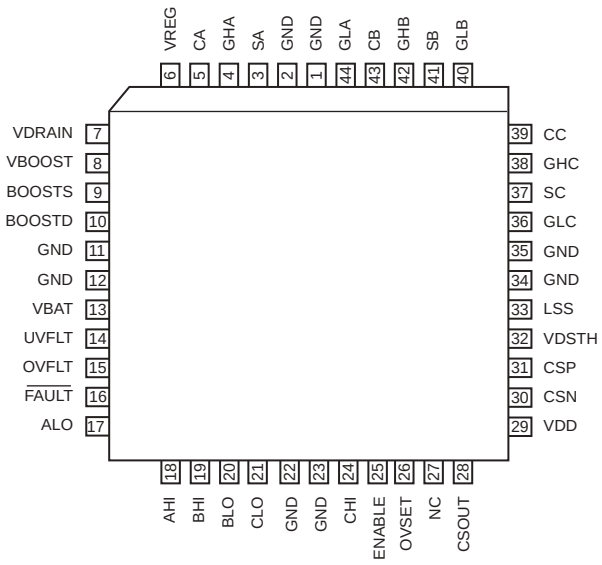
ENABLE	xLO	xHI	GLx	GHx	Mode of Operation
0	X	X	0	0	All gate drive outputs low
1	0	0	0	0	Both gate drive outputs low
1	0	1	0	1	High side on
1	1	0	1	0	Low side on
1	1	1	0	0	XOR circuitry prevents shoot-through

Fault Responses

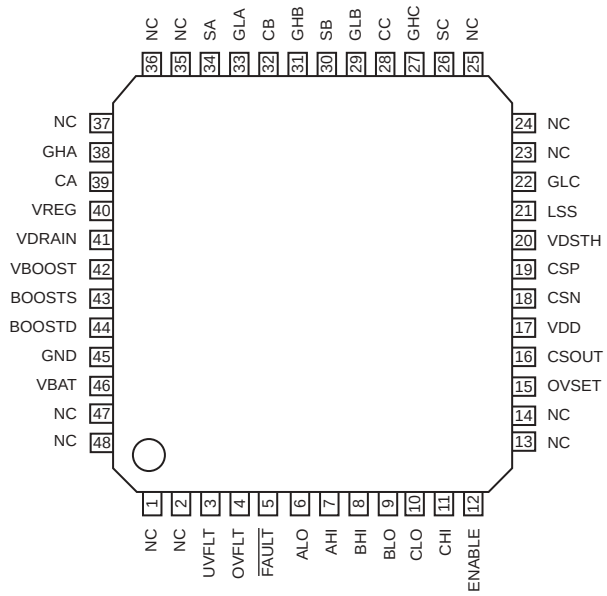
Fault Mode	ENABLE Input	$\overline{\text{FAULT}}$	OVFLT	UVFLT	Boost Reg.	V_{REG} Reg.	GHx	GLx
No Fault	X	1	0	0	ON	ON	①	①
Short-to-Battery	1②	0	0	0	ON	ON	①	①
Short-to-Ground	1③	0	0	0	ON	ON	①	①
Bridge (V_{DRAIN}) Fault	1④	0	0	0	ON	ON	①	①
V_{REG} Undervoltage	X	0	0	0	ON	ON	①	①
V_{BAT} Overvoltage	X	0	1	0	OFF⑤	ON	①	①
V_{BAT} Undervoltage⑥	X	0	0	1	OFF	OFF	0	0
V_{DD} Undervoltage⑥	X	0	Z	Z	OFF	OFF	0	0
Thermal Shutdown⑥	X	0	Z	Z	OFF	OFF	0	0

NOTES: x = "Little x "indicates A, B, or C phase.
X = "Capital X " indicates a "don't care".
Z = High-impedance state.
① = Depends on xLO input, xHI input, and ENABLE. See Input Logic table.
② = Short-to-battery can only be detected when the corresponding GLx = 1. This fault is not detected when ENABLE = 0.
③ = Short-to-ground can only be detected when the corresponding GHx = 1. This fault is not detected when ENABLE = 0.
④ = Bridge fault appears as a short-to-ground fault on all motor phases. This fault is not detected when ENABLE = 0.
⑤ = Off, only because $V_{BOOST} \approx V_{BAT}$ is above the voltage threshold of the regulator's voltage control loop.
⑥ = These faults are not only reported but action is taken by the internal logic to protect the A3935 and the system.

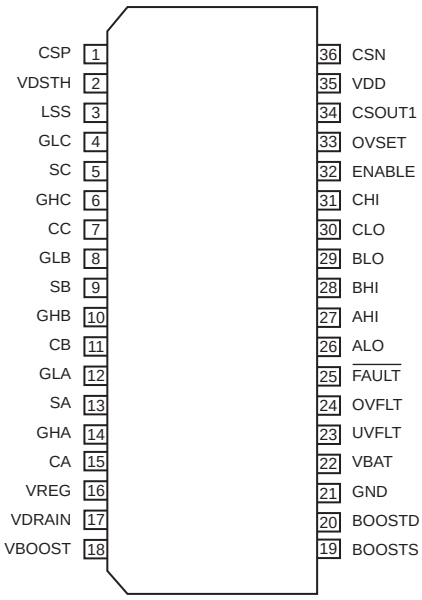
Package ED, 44-Pin PLCC



Package JP, 48-Pin LQFP



Package LQ, 36-Pin SOIC



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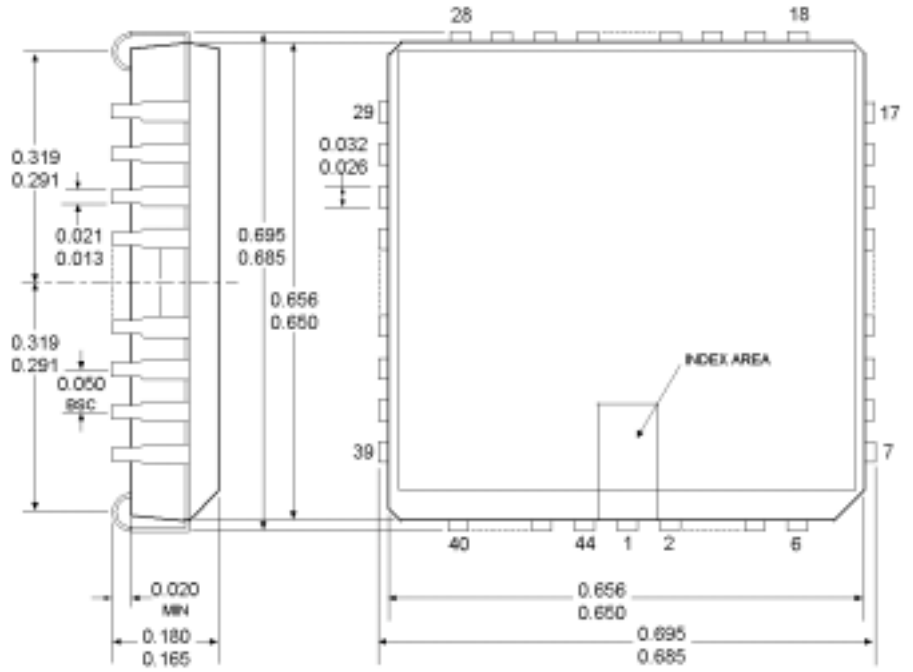
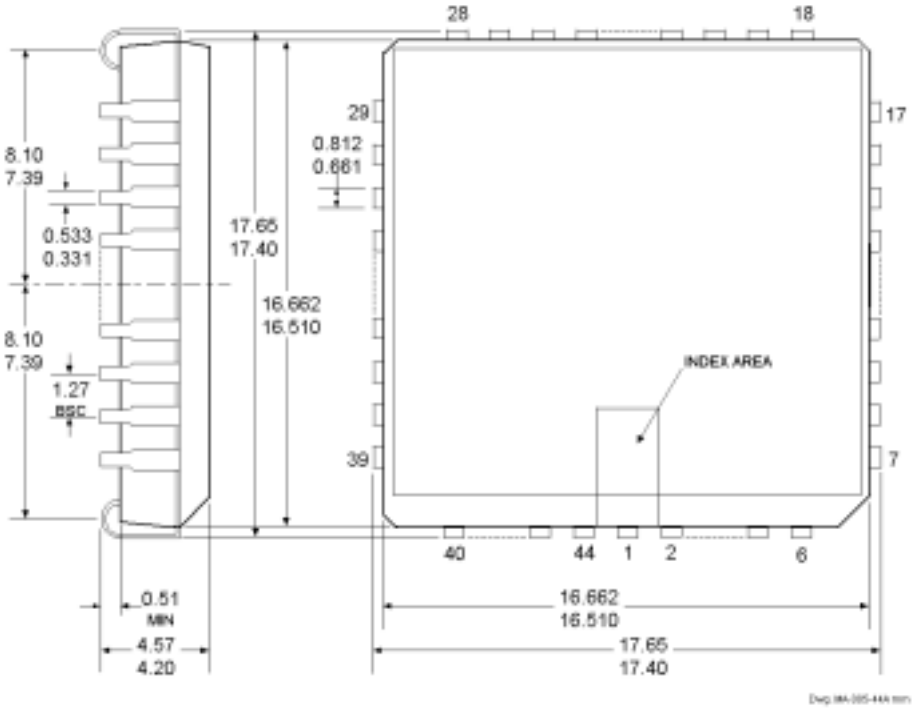
A3935KED (PLCC)



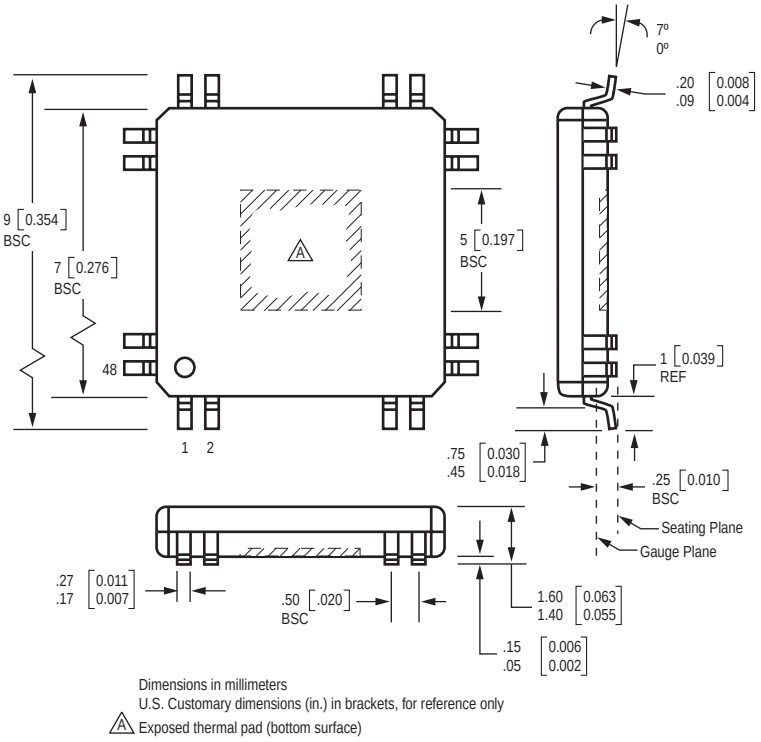
Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Webbed lead frame. Terminals 1, 2, 11, 12, 22, 23, 34, and 35 are internally one piece.
4. Supplied in standard sticks/tubes of 27 devices or add "TR" to part number for tape and reel.

A3935KJP (LQFP)



Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
A Exposed thermal pad (bottom surface)

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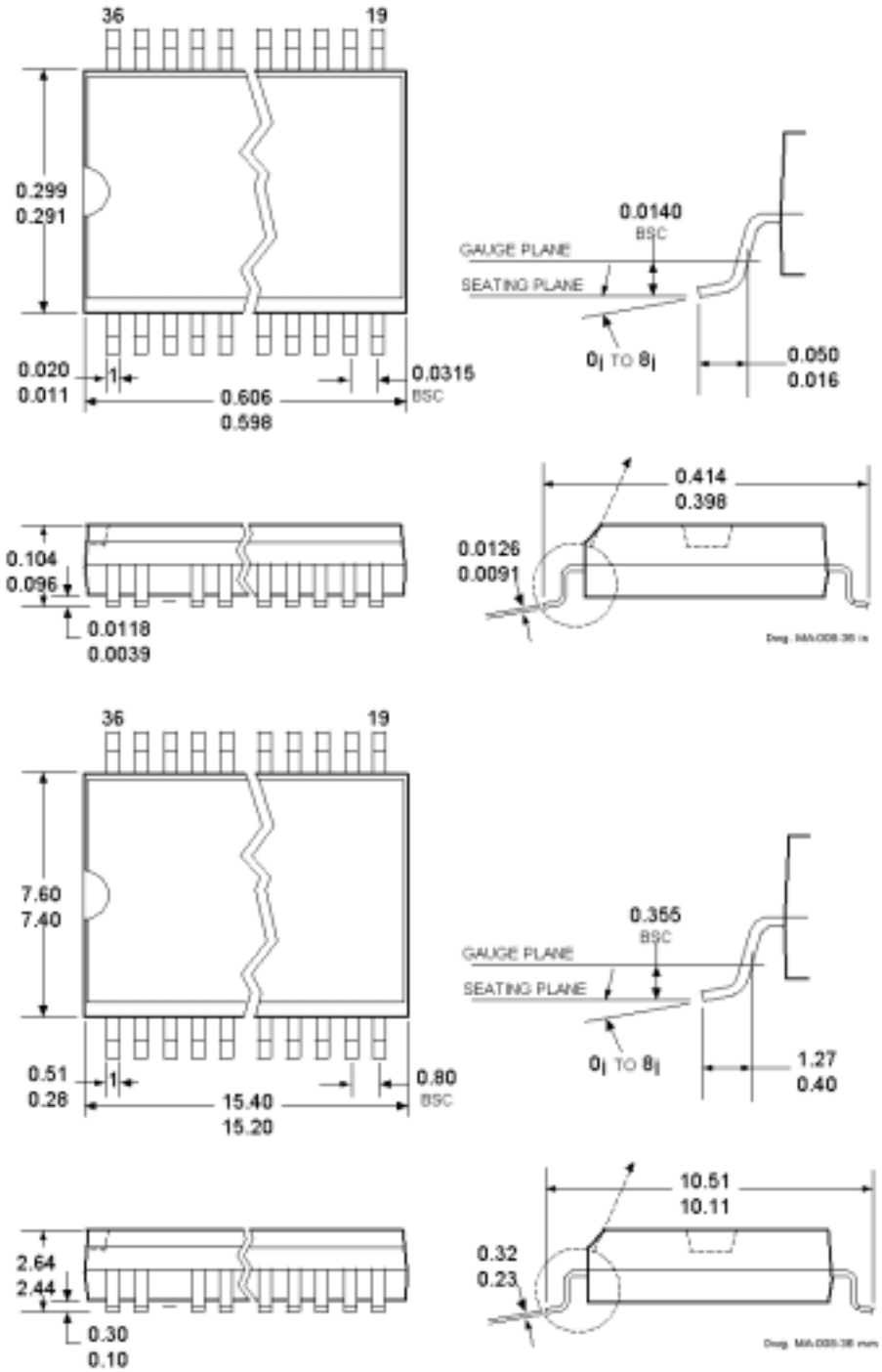
A3935KLQ (SOIC)



Dimensions in Inches
(for reference only)

Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

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